SUB-THRESHOLD LEAKAGE REDUCTION IN DOMINO LOGIC

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11-30-2010

Outline

- ✓ **Motivation and goal of this project**
- ✓ **Circuits implemented**
  - ➢ **2 input AND gate for data comparison**
  - ➢ **Carry generation circuit of a 16 Bits Carry look-ahead Adder**
- ✓ **Result and analysis**
  - ➢ **Our result**
  - ➢ **Comparison with data from publications**
- ✓ **Conclusion and references**

Power Consumption Roadmap

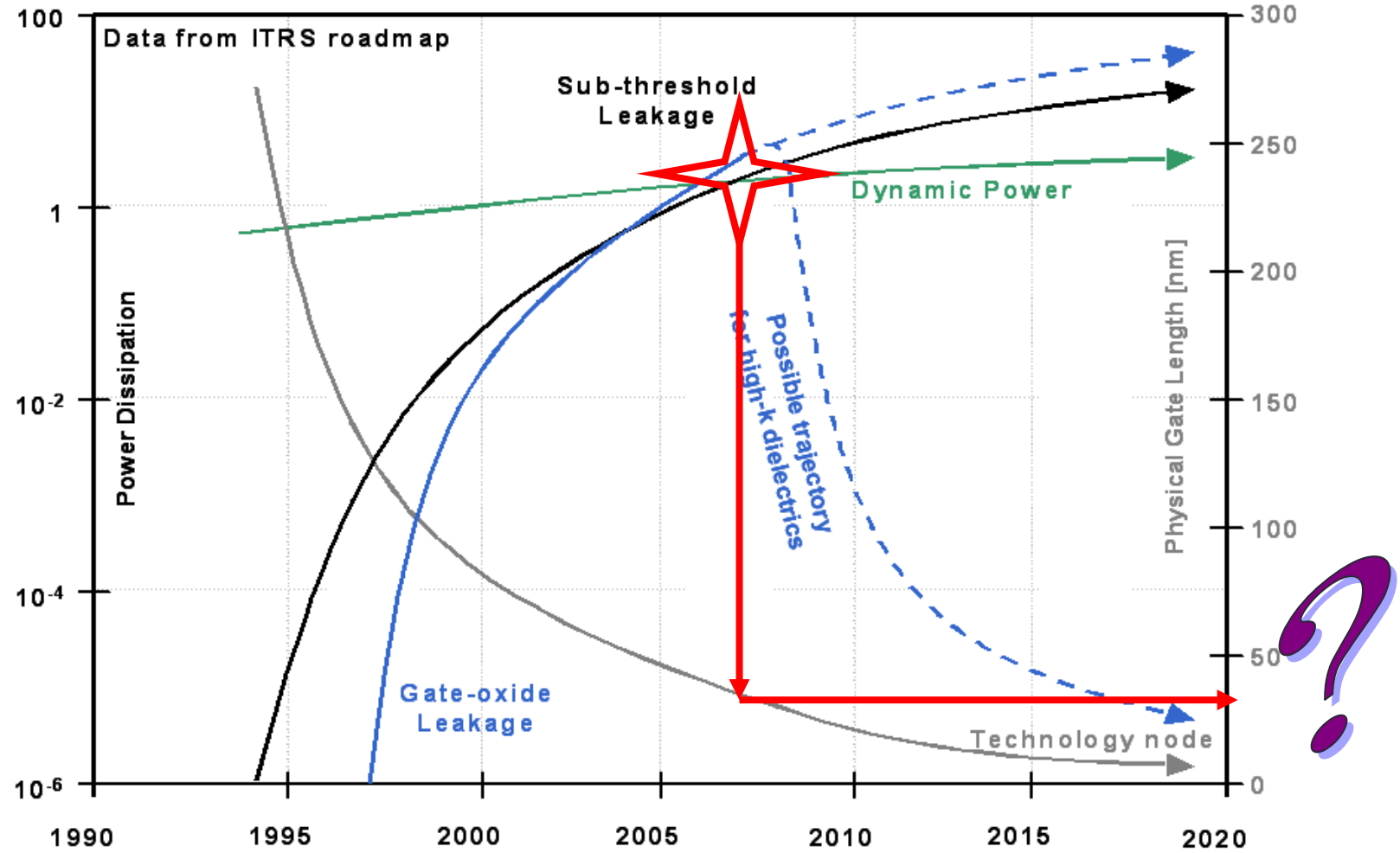


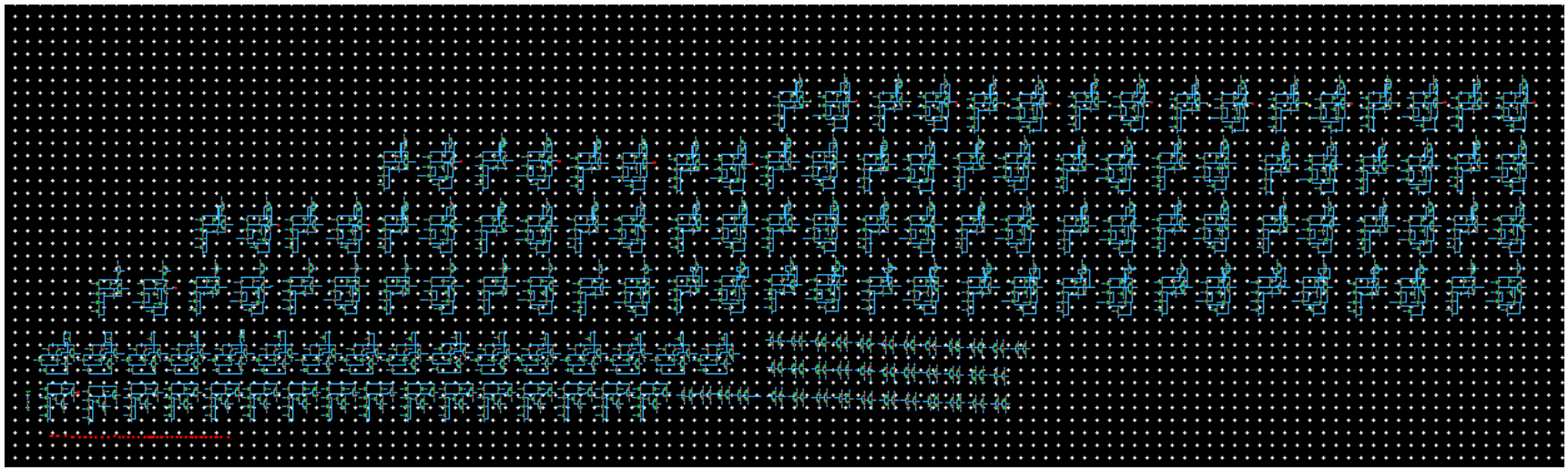
Figure1: ITRS Technology Roadmap: Power Trends.

Goal of this project

- Reduce sub-threshold leakage current by several techniques:
  - ✓Dual threshold voltage
  - ✓Sleep transistors
  - ✓Varying supply voltage
- Study the trend effect in CMOS technology
  - ✓Compare similar techniques realized in different scales: the 120nm, 65nm and 45nm technology
  - ✓Show the temperature trend in these techniques

Project Overview

- 2 Input AND Gate
- 16 Bit Carry look-ahead (CLA) adder:
  - 1507 transistors
  - 49 dot generators
  - 32 Propagators



CIRCUIT IMPLEMENTATION

2 INPUT DOMINO AND LOGIC

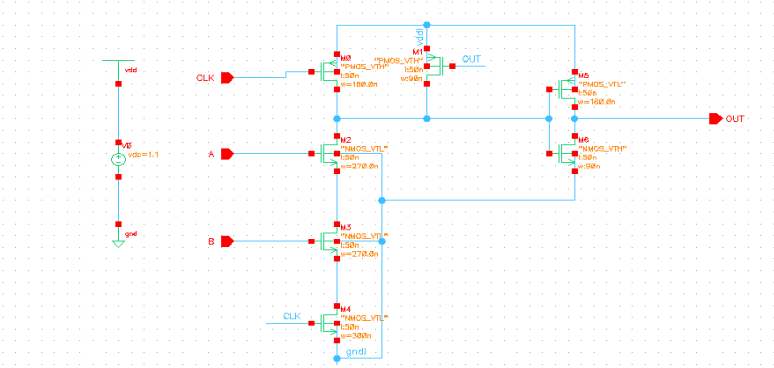


FIG STANDARD DUAL VT 2 INPUT DOMINO AND LOGIC CIRCUIT

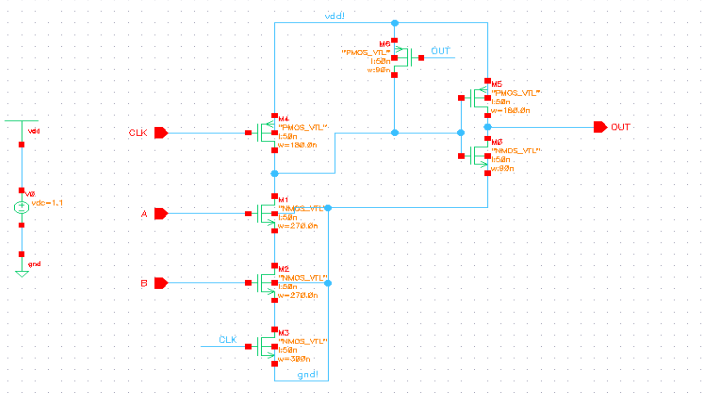


FIG STANDARD SINGLE VT (VTL) 2 INPUT DOMINO AND LOGIC CIRCUIT

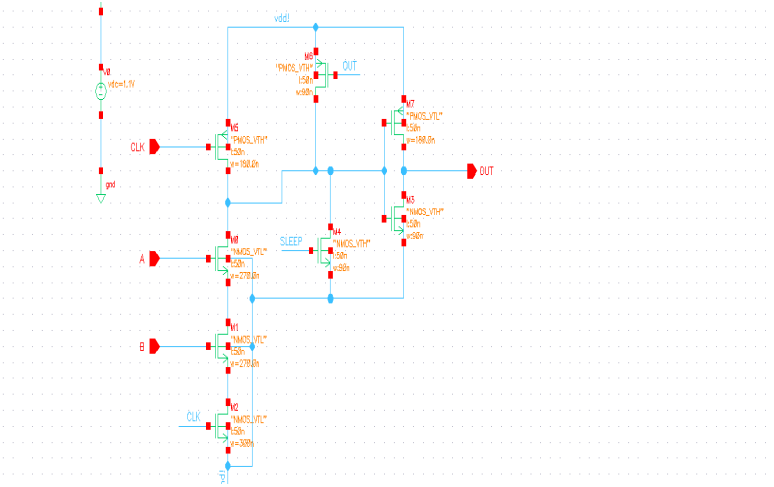


FIG DUAL VT 2 INPUT DOMINO AND LOGIC WITH SLEEP TRANSISTOR CIRCUIT

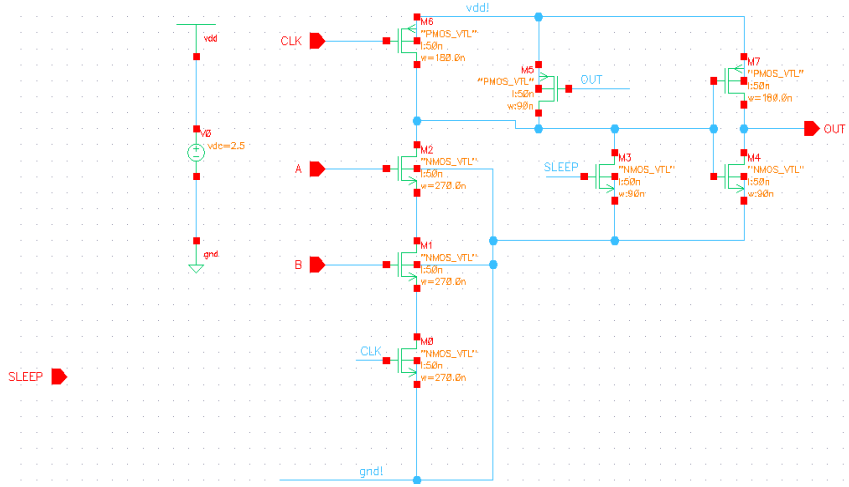
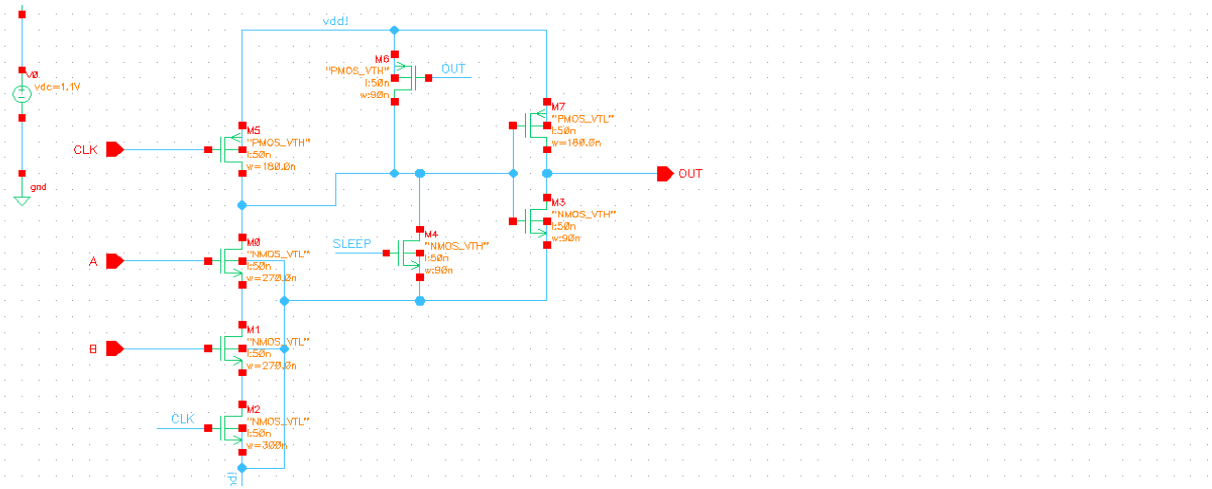


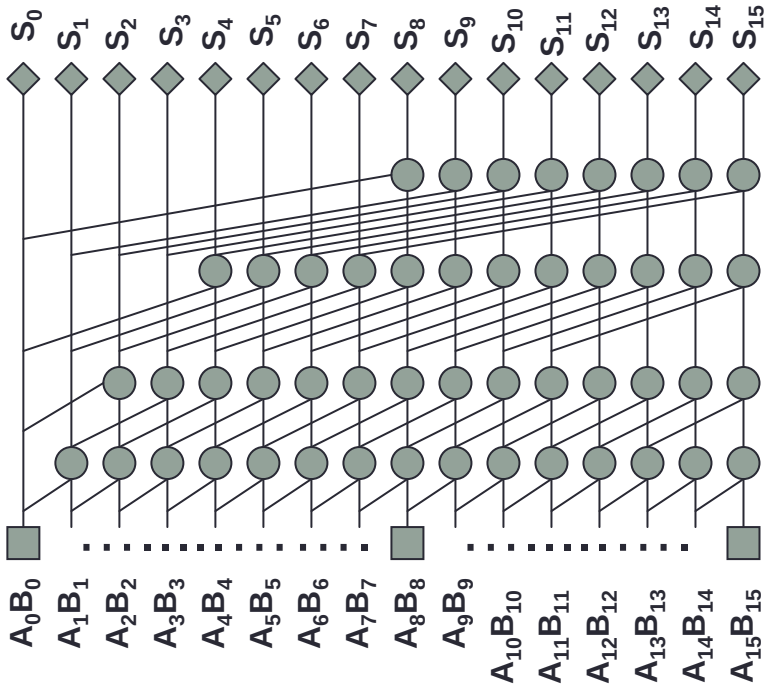
FIG SINGLE VT (VTL) 2 INPUT DOMINO AND LOGIC WITH SLEEP TRANSISTOR CIRCUIT

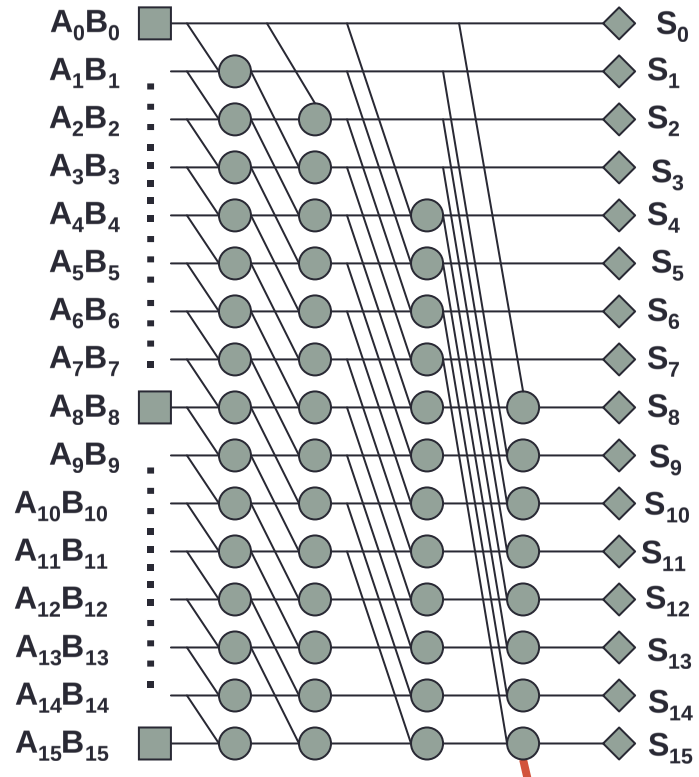
- By introducing a high vt sleep transistor between the dynamic node and ground in the dual vt circuit, it is possible to let the the high vt transistors to set the leakage current from vdd to ground.
- During the sleep mode, the clock and the sleep signals are set to ‘1’.
- This will cause the sleep transistor which is an NMOS be on which will cause a high dynamic node to go to ‘0’.
- This makes the high vt NMOS transistor of the output inverter to be off while the low vt PMOS transistor to be on.
- This will also put the high vt keeper transistor to be off thereby letting only the high vt transistors in the circuit to set the leakage current.



Kogge – stone 16 bit logarithmic carry look ahead

In order to see the benefit of introducing a high vt sleep transistor in a larger circuit, we implemented the carry generation circuit of a Kogge – stone logarithmic carry lookahead




A0B0
A1B1
A2B2
A3B3
A4B4
A5B5
A6B6
A7B7
A8B8
A9B9
A10B10
A11B11
A12B12
A13B13
A14B14
A15B15
S0
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S6
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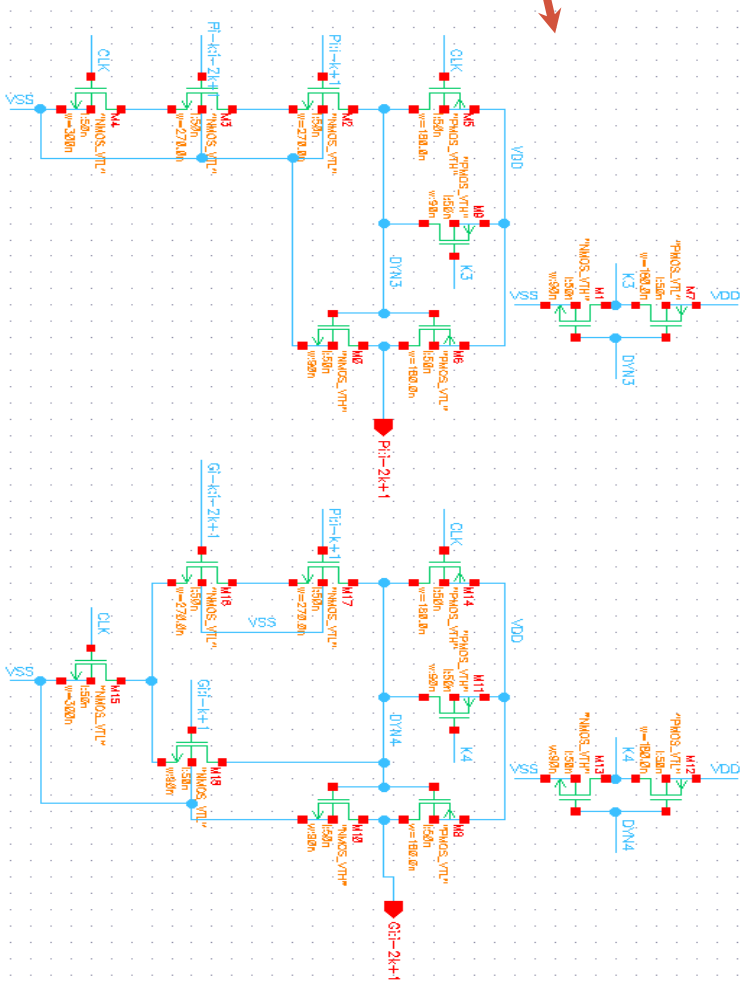
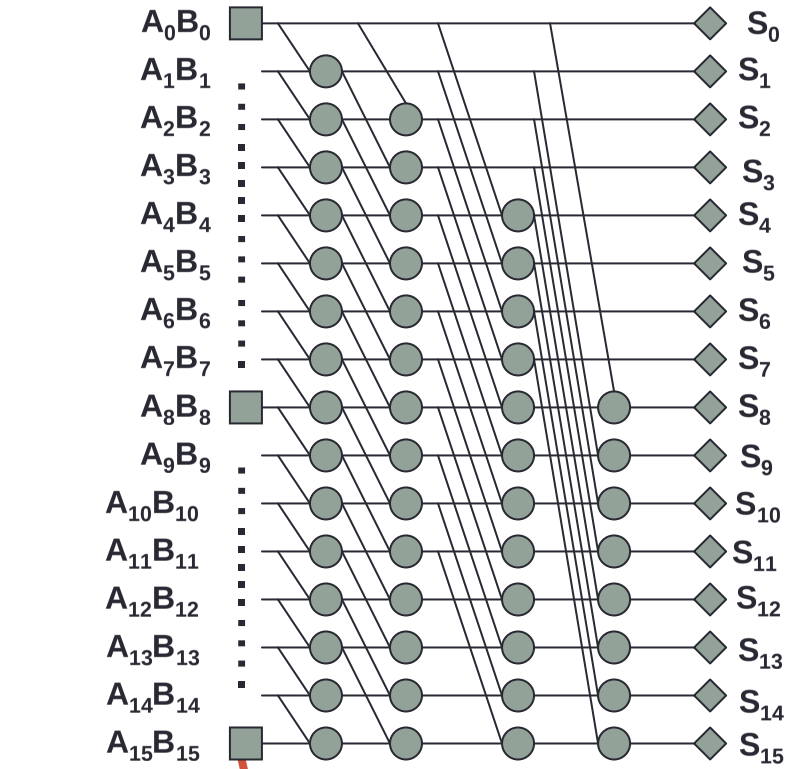
S9
S10
S11
S12
S13
S14
S15


CLK
VSS
VDD
DYN3
DYN4
K3
K4
Pi-k+1
Pi-k-2k+1
Gi-k+1
Gi-k-2k+1
Pi-2k+1
Gi-2k+1


A0B0
A1B1
A2B2
A3B3
A4B4
A5B5
A6B6
A7B7
A8B8
A9B9
A10B10
A11B11
A12B12
A13B13
A14B14
A15B15
S0
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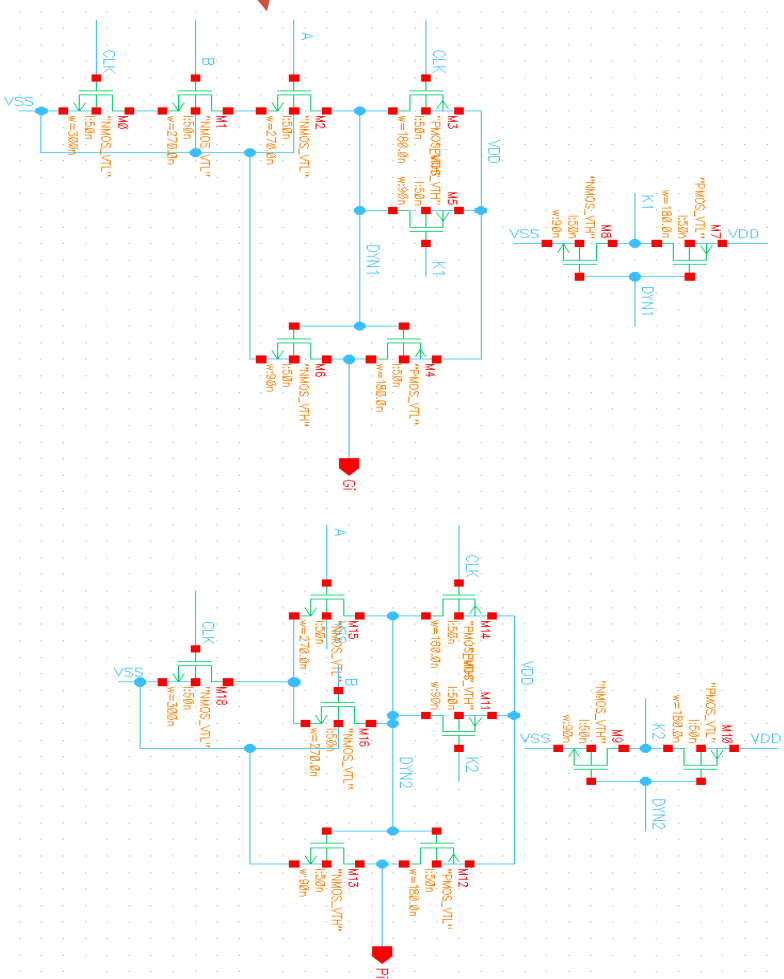
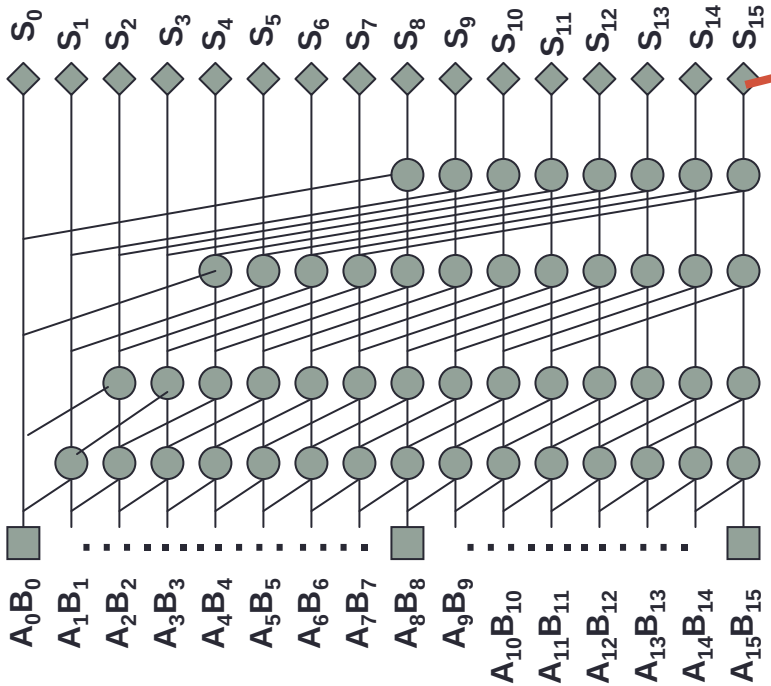
S15


CLK
A
B
VSS
VDD
DYN1
K1
K2
Gi
Pi



SUM GENERATION CIRCUIT NOT INCLUDED IN THIS CIRCUIT

RESULT AND ANALYSIS OF SIMULATIONS

Initial result from 2 input AND gate

- Dual VT with sleeper transistor suppress the leakage most
- 1.1 V is a better choice in terms of supply voltage

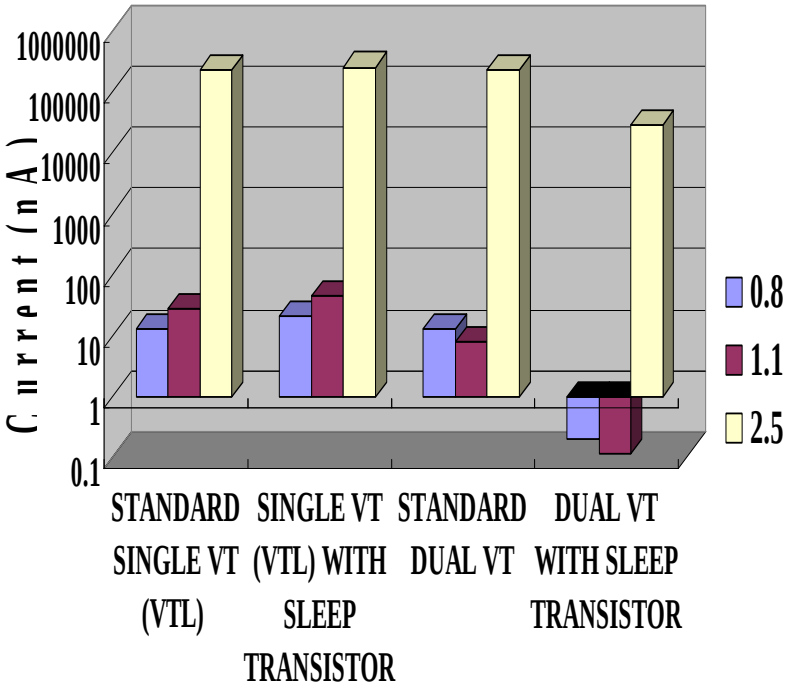
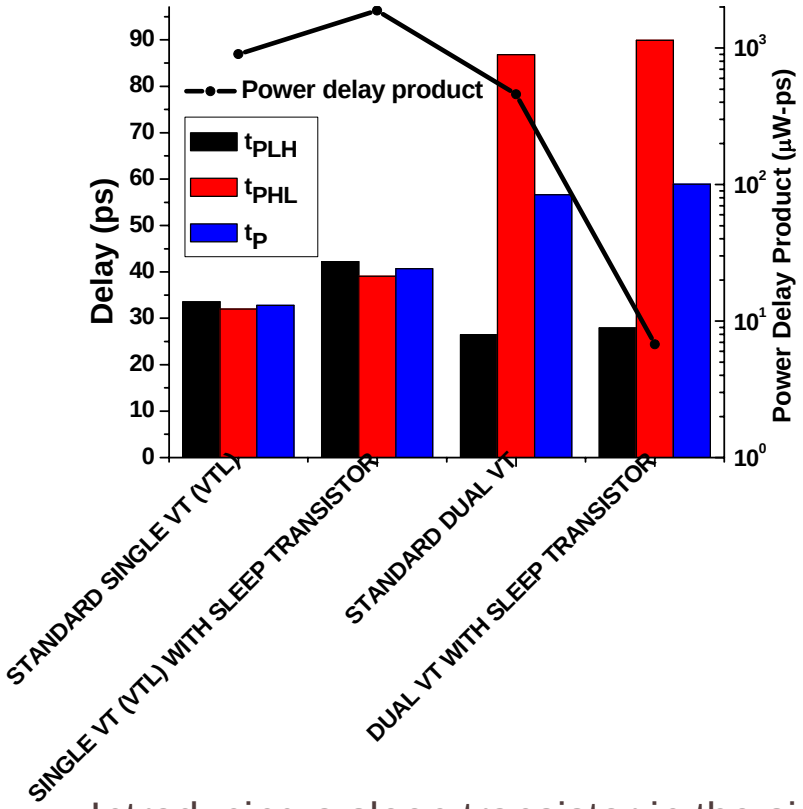


TABLE 1: LEAKAGE CURRENT OF A 2 INPUT DOMINO LOGIC WHILE VARYING THE VDD				
	STANDARD SINGLE VT (VTL)	SINGLE VT (VTL) WITH SLEEP TRANSISTOR	STANDARD DUAL VT	DUAL VT WITH SLEEP TRANSISTOR
VDD (V)	DRAIN CURRENT (nA)	DRAIN CURRENT (nA)	DRAIN CURRENT (nA)	DRAIN CURRENT (nA)
0.8	13.3726654	20.761804	12.7186	0.209038
1.1	27.5608654	46.18606	8.09745	0.11454073
2.5	233603.39	252252.23	227470	28019.133

Leakage Current for 2 input AND gate with various supply voltage in different circuits

Propagation Delay of the various technique



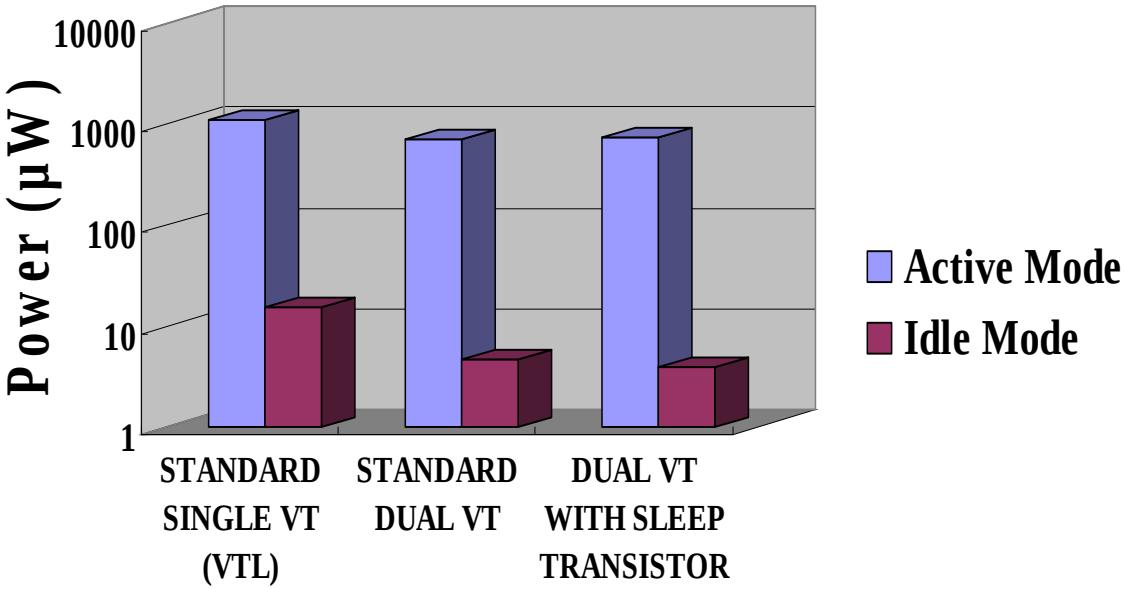
FOR A 2 INPUT AND DOMINO LOGIC			
	t_{PLH} (ps)	t_{PHL} (ps)	t_P (ps)
STANDARD SINGLE VT (VTL)	33.57	32	32.785
SINGLE VT (VTL) WITH SLEEP TRANSISTOR	42.25	39.1	40.675
STANDARD DUAL VT	26.5	86.8	56.65
DUAL VT WITH SLEEP TRANSISTOR	27.94	89.9	58.92

- Introducing a sleep transistor in the single vt (vtl) circuit contributes more leakage delay relative to the standard single vt (vtl) circuit. There is also an area overhead for this as an additional transistor has been introduced in the circuit.
- Dual VT with sleeper transistor suppress the leakage most

THE CARRY GENERATION CIRCUIT OF A 16 BIT CLA

Results

- Power consumption decreases by more than 100 times for dual VT implementation with and without sleep transistor for room temperature



	Idle Mode (µW)	Active Mode (µW)
STANDARD SINGLE VT (VTL)	15.33	1104
STANDARD DUAL VT	4.703	720.1
DUAL VT WITH SLEEP TRANSISTOR	3.9	741.2

Power dissipation in 16 Bit CLA adder for three different techniques

Temperature dependence of power dissipation applying different circuit techniques

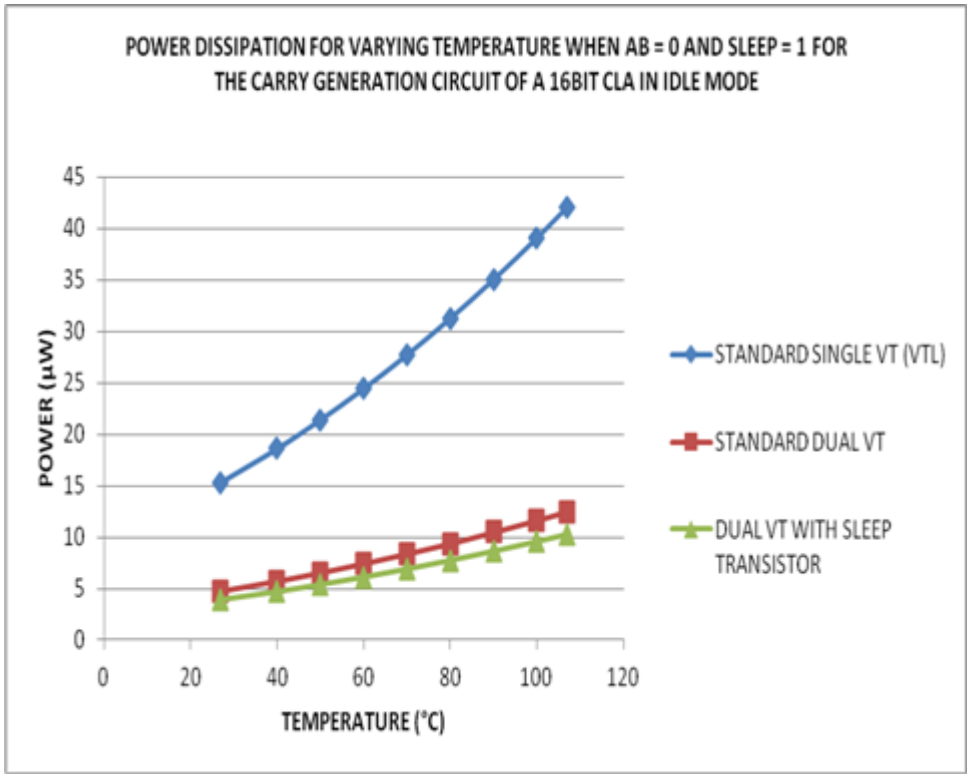
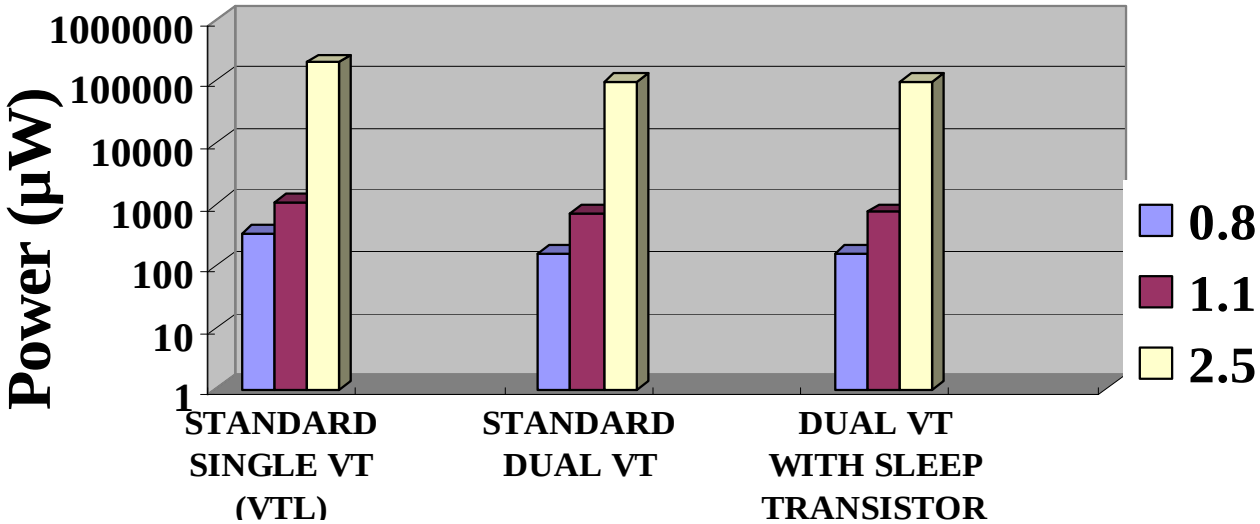


TABLE 2: POWER DISSIPATION FOR CARRY GENERATION BY 16 CLA WHEN AB = 00 AND SLEEP = 1 FOR VARYING TEMPERATURE

TEMPERATURE (°C)	STANDARD SINGLE VT (VTL) POWER (µW)	STANDARD DUAL VT POWER (µW)	DUAL VT WITH SLEEP TRANSISTOR POWER (µW)
27	15.33	4.703	3.9
40	18.6	5.679	4.706
50	21.4	6.505	5.388
60	24.43	7.398	6.123
70	27.71	8.359	6.913
80	31.24	9.36	7.758
90	35.02	10.48	8.657
100	39.06	11.65	9.611
107	42.05	12.5	10.31

Power dissipation is lower for the dual vt with sleep transistor with varying temperature. The same is true for its energy

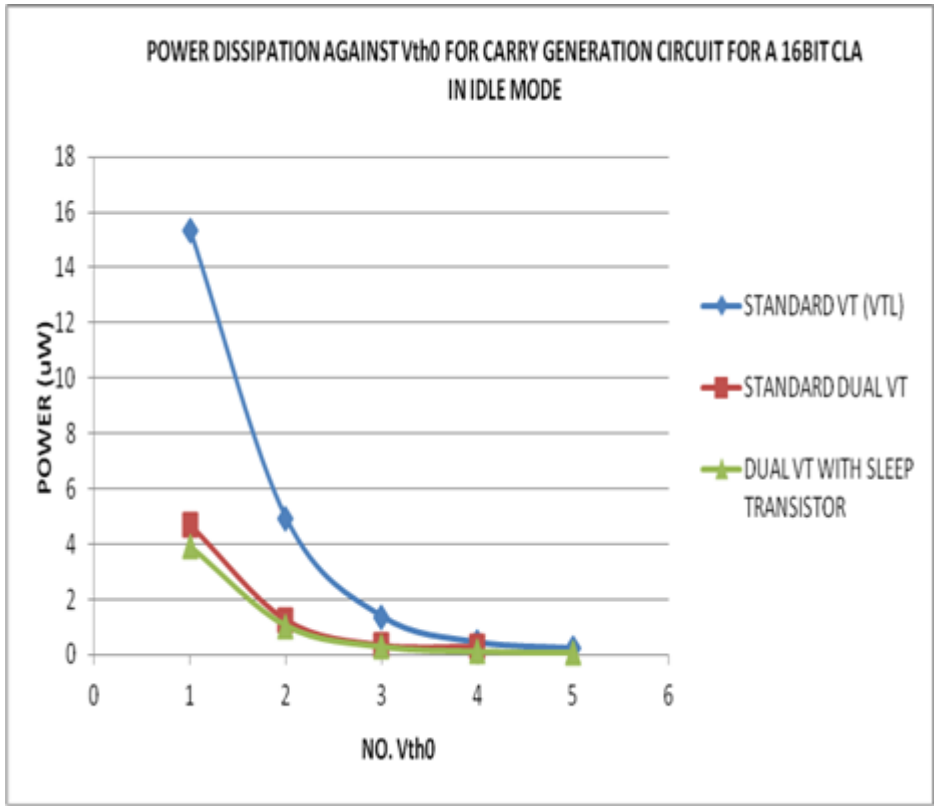
Power dissipation with varying V_{DD}



	STANDARD SINGLE VT (VTL)	STANDARD DUAL VT	DUAL VT WITH SLEEP TRANSISTOR
VDD (V)	AVERAGE POWER (µW)	AVERAGE POWER (µW)	AVERAGE POWER(µW)
0.8	329.8	156.8	159.6
1.1	1104	720.1	741.2
2.5	197700	99540	100000

- Power consumption at V_{DD}=1.1V decreases by two orders compared with that with V_{DD}=2.5V
- V_{DD}=0.8V consumes lower power but may have a speed problem

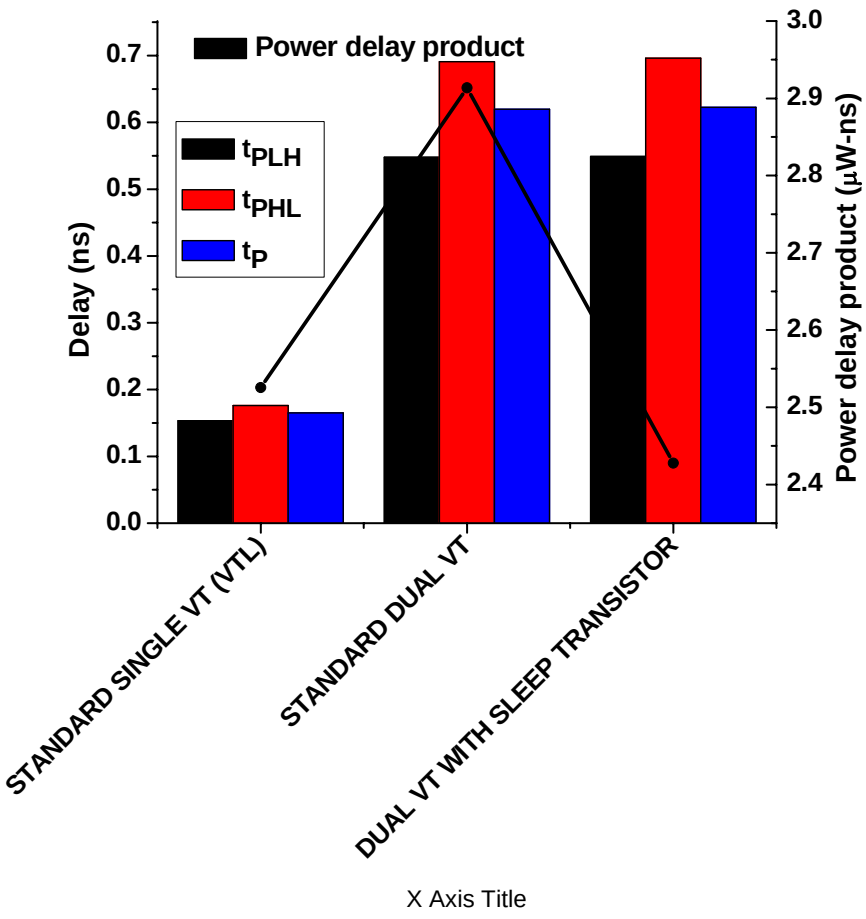
Power trend in terms of Low Vth0 transistors for idle mode operation at room temperature



2 Vth0 gives a decent drop in power

	V_{th0}				STANDARD VT (VTL)	STANDARD DUAL VT	DUAL VT WITH SLEEP TRANSISTOR
NO. Vth0	PMOS VTL	PMOS VTH	NMOS VTL	NMOS VTH	POWER (µW)	POWER (µW)	POWER (µW)
1	-0.2	-0.4	0.2	0.4	283.6	72.65	59.4
2	-0.302	-0.5044	0.322	0.6078	15.33	4.703	3.9
3	-0.35	-0.65	0.35	0.65	4.938	1.268	1.038
4	-0.4	-0.7	0.4	0.7	1.373	0.3579	0.282
5	-0.45	-0.75	0.45	0.75	0.437	0.3078	0.102
6	-0.5	-0.8	0.5	0.8	0.2119		0.06

Propagation delay of the carry generation circuit of the 16bit adder



CARRY GENERATION CIRCUIT OF A 16BIT CLA			
	t_{PLH} (ns)	t_{PHL} (ns)	t_P (ns)
STANDARD SINGLE VT (VTL)	0.1535	0.176	0.16475
STANDARD DUAL VT	0.548	0.691	0.6195
DUAL VT WITH SLEEP TRANSISTOR	0.549	0.696	0.6225

- Dual VT with sleeper transistor suppress the leakage most

Conclusion

- According to the overall performance, dual VT with sleep transistor has the best characteristics
- It is able to reduce the power dissipation and energy consumption during idle mode operation
- However during active mode operation, its power and energy is slightly higher than that of the standard dual VT circuit due to the additional sleep transistor introduced in the circuit. It is also slightly slower and has an area overhead compared to the standard dual VT
- In terms of supply voltage, 1.1 V provides decent leakage current while sustaining moderate speed
- Optimized VT is around 0.3V for PMOS and 0.5V for NMOS respectively for the 45nm technology as higher VTs makes the circuit slow even though it minimises the idle mode power and energy.
- Dual VT with sleep transistor also shows good temperature dependant characteristics

Reference

- Volkan Kursun, Eby G. Friedman, ‘Multi-voltage CMOS Circuit Design’, John Wiley & Sons Ltd, 2006
- James T. Kao and Anantha P. Chandrakasan, *‘Dual-threshold voltage techniques for low-power digital circuits’, IEEE journal of solid-state circuits’*, VOL. 35, NO. 7, July 2000
- Salendra. Govindarajulu and T. Jayachandra Prasad, *‘Design of low power, high speed, dual threshold voltage CMOS domino logic circuits with PVT Variations’*, International Journal of Electronic Engineer Research, Volume 2 Number 5, 2010
- Salendra. Govindarajulu and T. Jayachandra Prasad, *‘Energy-efficient reduced swing domino logic circuits in 65nm technology’*, International Journal of Engineering Science and Technology, Volume 2, 2010, 2248-2257

THANK YOU!

Questions?